UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,456	12/04/2001	Michael Kagan	3891-0101P	9182

7590 01/04/2007

Mark M. Friedman
Dr. Mark Friedman Ltd.
c/o Discovery Dispatch
9003 Florin Way
Upper Marlboro, MD 20772

EXAMINER	
DIVECHA, KAMAL B	
ART UNIT	**PAPER NUMBER**
2151	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/000,456	KAGAN ET AL.	
	Examiner	Art Unit	
	KAMAL B. DIVECHA	2151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,31-49 and 60-63* is/are pending in the application.

4a) Of the above claim(s) *20-30 and 50-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,31-49 and 60-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

Claims 1, 3-9, 11-12, 14-19, 31, 33-, 39, 41-42, 44-49 are pending in this application.

Claims 10, 40 and 60-63 have been cancelled in response filed on October 19, 2006.

Applicant's arguments filed October 19, 2006 in a request for continued examination (RCE) have been fully considered but they are not persuasive.

In response field, applicant argues in substance that:

a. Pettey et al., are silent concerning the internal architecture of various logics of bus router 306 (remarks, page 24).

In response to argument [a], Examiner respectfully disagrees.

In remarks, applicant presented the following correspondences between the prior art and the present claimed invention (See Remarks, page 23):

Present invention	TCA **202**
Host interface	PCI bus interfaces **312** and **316**
Network output port	IB MAC **308**
Network input port	IB MAC **308**
Outgoing packet generator	Bus router **306**
Incoming packet processor	Bus router **306**

On the other hand, claim 1 recites:

A network interface adapter, comprising:
a host interface, for coupling to a host processor;
an outgoing packet generator, adapted to generate an outgoing request packet for delivery to a remote responder responsive to a request submitted by the host processor via the host interface;
a network output port, coupled to receive the request packet from the outgoing packet generator, so as to transmit the outgoing request packet over a network to the remote responder;
a network input port, for coupling to the network so as to receive an incoming response packet from the remote responder, in response to the outgoing request packet sent thereto, and further to receive an incoming request packet sent by a remote requester; and
an incoming packet processor, coupled to the network input port so as to receive and process both the incoming response packet and the incoming request packet, and further coupled to cause the outgoing packet generator, responsive to the incoming request packet, to generate, in addition to the outgoing request packet, an outgoing response packet for transmission via the network output port to the remote requester;
wherein the outgoing request packet comprises an outgoing write request packet containing write data taken from a system memory accessible via the host interfiace, and
wherein the outgoing response packet comprises an outgoing read response packet containing read data taken from the system memory, in response to the incoming request packet, and
wherein the outgoing packet generator comprises a gather engine, which is coupled to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets via a common data flow path: and
wherein the incoming request packet comprises an incoming read request packet, and wherein responsive to the incoming read request packet, the incoming packet processor is adapted to prepare a read response work item in a memory location, and wherein the outgoing packet generator is coupled to read the read response work item from the memory location and, responsive thereto, to generate a read response packet.

In response to applicant argument above, applicant's attention is directed towards the claim above, which is also silent concerning the internal architecture of the various logics of Outgoing packet generator and Incoming packet processor.

Furthermore, It is not clear what other "various logics" applicant is referring to.

Therefore, applicant argument directed towards the distinction between the prior art and the claimed Invention, based on the feature above, is not persuasive.

b. Specifically, the limitation of claims 10 and 40 that distinguishes the present invention from the prior art cited by the Examiner is that the incoming packet processor prepares a read response work item, in a memory location, that is read by the outgoing packet generator to tell the outgoing packet generator how to generate the corresponding read response packet. In the embodiment of the present invention that is described in the specification, this read response work item is the "quasi-WQE" that is prepared by the TCU 52 in RDB 40 in response to the receipt of a RDMA read request from a remote requestor (See remarks, page 25).

In response to argument [b], Examiner respectfully disagrees.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "tell the outgoing packet generator how to generate the corresponding read response packet") are not recited in the rejected claim(s).

Applicant is reminded that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

If applicant's intention is directed towards the subject matter "Quasi-WQE", applicants is advised to distinctly and clearly disclose the subject matter in the independent claims.

c. It is emulation of the standard...that enables the present invention to use the same gather engine to gather data for both requestor and responder outgoing packet via the same data flow path (See remarks, page 25).

In response to argument [c], Examiner respectfully disagrees.

Again, the claim fails to disclose, teach or suggest "same gather engine to gather data for both the requestor and responder outgoing packet via the same data flow path".

Also, the gather engine or component has an inherent function of gathering the data from the memory location, in response to a read or write request using the common data flow because based on technical line of reasoning, when the gather engine is directly coupled to a memory, the gather engine utilizes the direct connection between the engine itself and the memory for either writing i.e. storing the data and/or reading, i.e. obtaining the data, from the memory.

Therefore, applicant's argument directed towards the distinction between the prior art and the claimed invention, based on the feature above, is not persuasive.

d. There is neither a hint nor a suggestion in the prior art of a channel adapter such as TCA 202 of Pettey et al., generating it own WQE equivalents, independently of its host, in response to packets received from remote requestors (Remarks, page 25-26).

In response to argument [d], Examiner respectfully disagrees.

First, the claim fails to teach, disclose or suggest A Channel Adapter generating its own WQE, i.e. a work queue entry equivalents, independently of its host, in response to packets received from remote requestors.

Secondly, Pettey clearly discloses a channel adapter comprising a bus router, wherein a bus router performs IB transport layer operations, such as work queue processing, memory registration, partition key management, etc. Furthermore, Pettey expressly teaches the process wherein "as a packet comes in from the IB fabric 114 through a MAC into a PMB 304, the packet header is placed by the Transaction Switch 302 into the header region 404 of the PMB 304 and packet payload is placed by the Transaction Switch 302 into the payload region 402 of the PMB 304. Conversely, when the TCA desires to transmit a packet on the IB fabric 114, the Bus Router 306 builds a packet header in the header region 404 of the PMB and a MAC 308 pulls the two packets portions from the PMB 304 and transmits it on the IB fabric 114 to its destination node...the Bus router will subsequently create an IB RDMA Write request packet in the PMB and cause the packet to be transmitted to the host that requested the data (See col. 8 L63 to col. 10 L9)".

Furthermore, Pettey discloses the process wherein "when a CPU 208 of fig. 2 desires to send the host a message, it submits a work request to the TCA 202 Send Queue. The TCA creates a Work Queue Entry (WQE) and places the WQE on the Send Queue. Among the WQE

types are RDMA Write WQE 762, RDMA Read WQE 763, DRDMA Write WQE 764, DRDMA Read WQE 765, and SEND WQE 766 (col. 11 L1-53)". Note that there is no involvement of the host in creating the Work Queue Entries.

As such, the TCA disclosed by the Pettey explicitly discloses the process wherein the TCA generates its own WQE equivalents, independently of its host, in response to packet received from the remote requestors.

Therefore, applicant argument's directed towards the distinction between the prior art and the claimed or disclosed invention, based on the feature above, is not persuasive.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 16, the phrase "such" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 3-9, 11-12, 14-19, 31, 33-39, 41-42 and 44-49 are rejected under 35 U.S.C. 103(a) as being obvious over Pettey et al. (U. S. Patent No. 6,594,712 B1) in view of Gasbarro et al. (hereinafter Gasbarro, U. S. Patent No. 6,948,004 B2).

As per claim 1, Pettey discloses a network interface adapter, comprising: a host interface for coupling to a host processor (fig. 2 item #206, fig. 18b item #308); an outgoing packet generator for delivery to a remote responder responsive to a request submitted by the host processor via the host interface col. 7 L65 to col. 8 L7, col. 14 L20-39, fig. 3 item #306); a network output port, coupled to receive the request packet from the output packet generator, so as to transmit the outgoing request packet over a network to the remote responder (col. 9 L1-5, fig. 3 item #308); a network input port, for coupling to the network so as to receive an incoming

response packet from the remote responder, in response to the outgoing request packet sent thereto, and further to receive an incoming request packet sent by a remote requester (fig. 3 item #308 and fig. 2 item #204); an incoming packet processor, coupled to the network input port so as to receive and process both the incoming response packet and the incoming request packet, and further coupled to cause the outgoing packet generator, responsive to the incoming request packet, to generate in addition to the outgoing request packet, an outgoing response packet for transmission via the network output port to the remote requester (col. 10 L4-9, col. 14 L40-54 and fig. 3 item #306), wherein the outgoing request packet comprises an outgoing write request packet containing write data taken from a system memory accessible via the host interface (fig. 18a: describes the process of RDMA WRITE operation; fig. 16 shows the I/O WRITE operation), wherein the outgoing response packet comprises an outgoing read response packet containing read data taken from the system memory in response to the incoming request packet (fig. 18a and fig. 16) and a scatter/gather list created by CPU (fig. 9), and wherein the incoming request packet comprises an incoming read request packet, and wherein responsive to the incoming read request packet, the incoming packet processor is adapted to prepare a read response work item in a memory location, and wherein the outgoing packet generator is coupled to read the response work item from the memory location and, responsive thereto, to generate a read response packet (fig. 15: describes an incoming read request packet, and col. 13 L58 to col. 14 L9, L40-65 and col. 15 L65 to col. 16 L6).

However Pettey does not explicitly disclose the process of gathering both the write data and the read data from the system memory for inclusion in the respective outgoing packets.

Gasbarro, from the same field of endeavor, explicitly discloses an interface adapter (fig. 7) comprising a gather engine providing a gather list describing virtual addresses to fetch outgoing whether it's a read or write data from local system memory for inclusion in the outgoing packets via a common data flow path (col. 8 L10-34, col. 11 L14-45, col. 12 L64 to col. 13 L5, col. 15 L20-67, col. 21 L16-56: please also note that it is the inherent function of the gather engine to gather the data in response to either write or read request regardless of incoming and outgoing packets).

Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro, in order to gather both the write data and the read data from the system memory for inclusion in the respective outgoing packets, since Gasbarro teaches the process of gathering outgoing data from the system memory.

One of ordinary skilled in the art would have been motivated because it would have enabled the process of fetching outgoing data from system memory whether it's a read or write data (Gasbarro, col. 8 L28-34).

As per claim 3, Pettey discloses an adapter wherein to submit the request, the host processor writes a request descriptor indicative of the write data to a first memory location, and wherein to cause the outgoing packet generator to generate the outgoing response packet, the incoming packet processor writes a response descriptor indicative of the read data to a second memory location (this approach is known as double buffering, col. 11 L18 to col. 12 L45 and fig. 7b) and wherein the WQE includes SGL local address field for specifying the physical address in local memory of a scatter/gather list, however Pettey does not disclose a process adapted to read

information from the descriptors and to gather the read data and the write data responsive thereto.

Gasbarro discloses a scatter/gather engine adapted to read information from the indicators or descriptors and to gather or fetch the read data and the write data (col. 8 L28-41).

Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro, in order to read information from the descriptors and to gather or fetch the write data and the read data from the system memory, since Gasbarro teaches the process of gathering outgoing data from the system memory.

One of ordinary skilled in the art would have been motivated because of the same reasons as set forth in claim 1.

As per claim 4, Pettey discloses an interface adapter wherein the outgoing packet generator comprises a plurality of schedule queues (fig. 7a block #108), and is adapted to generate the outgoing request packet (fig. 16) and the outgoing response packet responsive to respective entries placed in the queues (fig. 18a item #1808, 1822, fig. 22a item #2224, 2226 and fig. 15).

As per claim 5, Pettey discloses an interface adapter wherein the network input and output ports are adapted to receive and send the incoming and outgoing packets, respectively, over a plurality of transport service instances, and wherein the outgoing request packet and the outgoing response packet are associated with respective instances among the plurality of transport service instances (fig. 7a item #108), and wherein the outgoing packet generator is adapted to assign the transport service instances to the queues based on service parameters of the instances, and to place the entries in the schedule queues corresponding to the transport service

instances with which the incoming and outgoing packets are associated (col. 8 L2-26, col. 11 L1-36 and col. 14 L10-54 and col. 17 L20-40).

As per claim 6, Pettey discloses an adapter wherein the outgoing packet generator comprises one or more execution engines, which are adapted to generate the outgoing request packet and the outgoing response packet responsive to a list of work items respectively associated with each of the transport service instances (col. 1 L54 to col. 2 L21, col. 7 L65 to col. 8 L7, col. 11 L18-53), however Pettey does not disclose a scheduler, which is coupled to select the entries from the queues and to assign the instances to the execution engines for execution of the work items responsive to the service parameters.

Gasbarro discloses an adapter comprising a scheduler for scheduling the next virtual interface to the context manager and supporting priority of traffic for data packets associated with send Queue and Receive Queue of the work queue pair (col. 15 L50-58).

Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view Gasbarro, in order to include a scheduler for selecting the entries from the queues and to assign the instances to the execution engines for execution of the work items responsive to the service parameters.

One of ordinary skilled in the art would have been motivated because a scheduler would have supported the priority of traffic for data packets associated with Send queue and Receive queue of the work queue pair (Gasbarro, col. 15 L50-55).

As per claim 7, Pettey discloses an adapter wherein the transport service instances comprise queue pairs (fig. 7a-7b: shows plurality of queues including queue pairs).

As per claim 8, Pettey discloses an adapter wherein the outgoing packet generator comprises one or more control registers to which the host processor and incoming packet processor write in order to place the entries in the queues (Pettey, col. 17 L20-56), however Pettey does not explicitly disclose the one or more register to be a doorbell registers.

Gasbarro, from the same field of endeavor explicitly discloses a channel adapter comprising one or more doorbell registers (col. 15 L20-50).

Therefore it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey in view of Gasbarro, in order to replace the one or more control registers with the doorbell registers, since Gasbarro teaches and discloses the usage of doorbell registers.

One of ordinary skilled in the art would have been motivated because doorbell registers allows software the capability to enable automatic event generation, and making doorbell registers memory mapped allows applications the ability to write those registers thereby controlling event generation (Gasbarro, col. 15 L20-32).

As per claim 9, Pettey discloses an adapter wherein the incoming request packet comprises a write request packet carried over the network on a reliable transport service, and wherein responsive to the incoming write request packet, the incoming packet processor is adapted to add an entry to the entries placed in the queues, such that responsive to the entry, the outgoing packet generator generates an acknowledgement packet (col. 19 L55 to col. 20 L33).

As per claim 11, Pettey discloses the process of receiving a read request (fig. 15 item #1000); the process of receiving a write request (fig. 16 item #1000); and the process of conveying or sending the write data to the host interface (fig. 15 item #1100), however Pettey

does not disclose the process of receiving an incoming write request packet containing write data to be written to a system memory accessible via the host interface after receiving the incoming read request packet, and the process of conveying the write data to the host interface without waiting for execution of the read response work item. But it would have been obvious to a person of ordinary skilled in the art at the time the invention was made to modify Pettey (i.e. modify Pettey's figure 15 and 16 so that the incoming packet processor of the adapter (see the rejected claim 1) is configured so that the write request work queue entry is executed first with respect to read response work queue entry) in order to convey the write data to the host interface without waiting for execution of the read response work item, since Pettey teaches receiving incoming write request, receiving incoming read request packet, executing both of the requests, and conveying the write data to the host interface. One of ordinary skilled in the art would have been motivated because it would have improved the efficiency and enhanced the performance of the interface adapter.

As per claim 12, Pettey discloses an adapter wherein the incoming packet processor is configured so that when it receives an incoming write request packet containing write data to be written to a system memory accessible via the host interface before receiving the incoming read request packet, it prevents execution of the read response work item until the write data have been written to the system memory (col. 21 L12 to col. 22 L6).

As per claim 14, Pettey discloses an adapter wherein the outgoing packet generator is adapted, upon generating the outgoing request packet, to notify the incoming packet processor to await the incoming response packet so as to write a completion message to the host interface when the awaited packet is received (col. 20 L17-32).

As per claim 15, Pettey discloses an adapter wherein the incoming request packet comprises an incoming read request packet specifying data to be read from a system memory accessible via the host interface, and wherein the incoming packet processor is adapted to write a response descriptor to a memory location indicating the data to be read from the system memory responsive to the read request packet (fig. 18a item #1822), and wherein the outgoing packet processor is adapted to read the response descriptor from the memory location and, responsive thereto, to read the indicated data and to generate the outgoing response packet containing the indicated data (fig. 18a item #1832; col. 15 L5 to col. 16 L6).

As per claim 16, Pettey discloses an adapter wherein the incoming read request packet is one of a plurality of incoming read request packets, and wherein the incoming packet processor is adapted to write the response descriptor to the memory location as part of a list of such descriptors, responsive to which the outgoing packet processor is adapted to generate the outgoing response packet as part of a sequence of such packets (fig. 19a, fig. 20 and fig. 9; col. 23 L20 to col. 24 L27; col. 11 L18-37).

As per claim 17, Pettey discloses an adapter wherein the network input and output ports are adapted to receive and send the incoming and outgoing packets, respectively, over a plurality of transport service instances, and wherein the incoming packet processor is adapted to prepare the list of the response descriptors for each of the instances as a part of a response database held for the plurality of the instances in common (fig. 3 item #308, fig. 19b item #508, and fig. 23).

As per claim 18, Pettey discloses an adapter wherein the transport service instances comprise queue pairs (fig 7a item #712).

As per claim 19, Pettey discloses an adapter wherein the request comprises a write request, which is submitted by the host processor by generating a request descriptor indicating further data to be read from the system memory for inclusion in the outgoing packet (fig. 10), and wherein the output packet generator is adapted to read the request descriptor and, responsive thereto, to generate the outgoing request packet as a write request packet containing the indicated further data (fig. 18a item #1832; col. 12 L58 to col. 13 L18, col. 15 L17-31 and fig. 16).

As per claims 31, 33-39, 41-42 and 44-49, they do not teach or further define over the limitations in claims 1, 3-9, 11-12, 14-19. Therefore claims 31, 33-39, 41-42 and 44-49 are rejected for the same reasons as set forth in claims 1, 3-9, 11-12 and 14-19.

Additional References

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Beukema et al., U. S. Patent No. 6,578,122 B2.

b. Avery, U. S. Patent No. 6,611,883 B1.

c. Thomas et al., U. S. Patent No. 5,922,046.

d. Coffman et al., U. S. Patent No. 6,718,370 B1.

Conclusion

Please Note: This Action is made Non-Final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAMAL B. DIVECHA whose telephone number is 571-272-5863. The examiner can normally be reached on Increased Flex Work Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarni Maung can be reached on 571-272-3939. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kamal Divecha
Art Unit 2151
December 22, 2006.

SUPERVISORY PATENT EXAM